METHODS AND SYSTEMS FOR SENSING AND COMPENSATING FOR PROCESS, VOLTAGE, TEMPERATURE, AND LOAD VARIATIONS

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Application No. 10/178,272, filed June 25, 2002, titled "Methods and Systems for Sensing and Compensating for Process, Voltage, Temperature, and Load Variations," (allowed), which claimed priority to U.S. Provisional Application No. 60/343,582, filed January 2, 2002, titled "Methods and Systems for Sensing and Compensating for Process, Voltage and Temperature Variations," both of which are incorporated herein by reference in their entireties.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention is directed to methods and systems for sensing and compensating for process, voltage, and/or temperature ("PVT") variations in integrated circuits ("ICs") and loads and, more particularly, for sensing and compensating for PVT variations in IC's that are impedance matched to loads.

Related Art

[0003] Integrated circuits ("ICs") need to interface with widely varying loads, such as 40 ohm to 100 ohm transmission lines. In order to reduce voltage waveform reflections and consequent loss of signal integrity, output impedances of ICs should match load impedances.

[0004] IC characteristics and load characteristics can vary due to process (e.g., manufacturing process), voltage, and/or temperature ("PVT") variations. ICs that are fabricated with narrower track widths tend to be more susceptible to

PVT variations. PVT variations adversely affect circuit characteristics, such as impedances and rise and fall times of waveforms.

[0005] What are needed are methods and systems for maintaining circuit and/or signal characteristics, such as impedance matching characteristics and rise and fall time characteristics, over a range of PVT variations.

SUMMARY OF THE INVENTION

[0006] The present invention is directed to methods and systems for maintaining circuit and/or signal characteristics, such as impedance matching characteristics and rise and fall time characteristics, over a range of PVT variations. The invention is useful, for example, where an IC output is coupled to a load.

[0007] In accordance with the invention, a PVT compensating circuit senses one or more circuit and/or signal characteristics at an output pad or terminal. When the one or more circuit and/or signal characteristics are affected by PVT variations in the IC and/or load, the PVT compensating circuit controls a variable output drive to maintain the one or more circuit and/or signal characteristics within a desired or predetermined range. The PVT compensating circuit is designed to compensate over a range of PVT variations.

[0008] In an embodiment, the PVT compensating circuit senses a rate of voltage change over time (i.e., dV/dt), of an output signal at the output terminal. During state transitions of the output signal, the output signal is adjusted as needed to maintain a desired, or pre-determined, rate of voltage change. As a result, the present invention enables control of output drive dependent on load.

[0009] In an embodiment, the PVT compensating circuit and the variable output drive are part of an output circuit coupled between an IC and an output terminal. The output circuit further includes an output impedance. When neither the circuit nor the load are substantially affected by PVT variations,

the output impedance substantially matches the load impedance and the output signal characteristic(s) of interest are generally within a desired or predetermined range. When the IC and/or the load are affected by PVT variations, the PVT compensating circuit senses the affect and adjusts the variable output drive to make suitable corrections. In an embodiment, the output drive adjusts rise and/or fall times of an output waveform. Alternatively, or additionally, the variable output drive adjusts the output impedance of the output circuit.

[0010] In an embodiment, the output signal is initially driven by a primary output drive. Additional compensation is added as needed by the variable output drive. In an alternative embodiment, output signal is driven solely by the variable output drive circuit.

[0011] In an embodiment, the primary output drive and/or the variable output drive include impedances that, alone or in combination with other impedances, substantially match the load impedance.

[0012] In an embodiment, the output circuit is implemented on the same die or wafer as the IC. In an embodiment, the output circuit is implemented with process technology that is less susceptible to PVT variations. For example, in an embodiment, one or more portions of the output circuit are implemented using wider path widths than those used in the IC and/or load.

[0013] Further features and advantages of the present invention, as well as the structure and operation of various embodiments of the present invention, are described in detail below with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0014] The present invention will be described with reference to the accompanying drawings, wherein like reference numbers indicate identical or functionally similar elements. Also, the leftmost digit(s) of the reference numbers identify the drawings in which the associated elements are first introduced.

[0015] FIG. 1 is a high-level block diagram of an output circuit in accordance with an aspect of the present invention.

[0016] FIG. 2 is a block diagram of an example embodiment of the output circuit illustrated in FIG. 1.

[0017] FIG. 3 is a circuit diagram of an example embodiment of the output circuit illustrated in FIG. 2.

[0018] FIG. 4 is another circuit diagram of an example embodiment of the output circuit illustrated in FIG. 2.

[0019] In FIG. 5 is another circuit diagram of an example embodiment of the output circuit illustrated in FIG. 2.

[0020] FIG. 6 is another circuit diagram of an example embodiment of the output circuit illustrated in FIG. 2.

[0021] FIG. 7 is another circuit diagram of an example embodiment of the output circuit illustrated in FIG. 2.

[0022] FIG. 8 is another circuit diagram of an example embodiment of the output circuit illustrated in FIG. 2.

[0023] In FIG. 9 is a process flowchart for implementing the present invention.

DETAILED DESCRIPTION OF THE INVENTION

I. Introduction

[0024] The present invention is directed to methods and systems for maintaining circuit and/or signal characteristics, such as impedance matching characteristics and rise and fall time characteristics, over a range of PVT variations.

[0025] FIG. 1 is a high-level block diagram of an output circuit 100 in accordance with the present invention. The output circuit 100 includes a PVT compensating circuit 106 and a variable output drive 108. The output circuit 100 is coupled between an input terminal 102 and an output terminal 104. The input terminal 102 couples the output circuit 100 to an IC core 110. The IC

core 110 can be any of a variety of types of integrated circuitry. The IC core 110 outputs a data signal 112, which is propagated through the output circuit 100 to the output terminal or pad 104. The output pad 104 is coupled to a load 114 having a load impedance.

[0026] The output circuit 100 further includes impedance matching circuitry (not shown in FIG. 1) that substantially matches the output impedance of circuit 100 to the load impedance. The impedance matching circuitry helps to insure that signal characteristics at the output terminal 104 are within a desired range. PVT variations, however, can affect the signal characteristics.

[0027] The PVT compensating circuit 106 monitors/senses an output signal 120 at the output terminal 104 for PVT variations. PVT variations can be due to PVT variations in the IC core 110, the output circuit 100, and/or the load 114. The PVT compensating circuit 106 outputs a control signal 116 that controls the variable output drive 108. The variable output drive 108 generates a compensation output signal 118, which compensates for detected PVT variations. In the example of FIG. 1, the compensation output signal 118 is provided directly to the output terminal 104. Alternatively, the compensation output signal 118 is provided to the output terminal 104 through an impedance resistance, as described below.

[0028] PVT variations can affect rise and fall times of the output signal 120. In an embodiment, the PVT compensating circuit 106 senses rising and falling edges of the output signal 120 at the output terminal 104, and controls the variable output drive 108 to compensate the rising and falling edges with additional drive as needed.

[0029] In an embodiment, the PVT compensating circuit 106 senses changes in voltage with respect to time ("dV/dt") and varies the control signal 116 in proportion to the rate of change (dV/dt). In an embodiment, the PVT compensating circuit 106 varies the control signal 116, and thus the variable output drive 108, inversely proportional to the dV/dt. In other words, at higher dV/dt, the variable output drive 108 provides little, if any, compensation. As the dV/dt decreases, the variable output drive 108 increases the compensation.

[0030] In an embodiment, when the output signal 120 at the output terminal 104 should be at steady state, the output circuit 100 provides no compensation. Alternatively, when the output signal should be at steady state, the output circuit 100 maintains a constant level of compensation.

[0031] FIG. 2 is a high-level block diagram of an output circuit 200 in accordance with an aspect of the present invention. The output circuit 200 is an example embodiment of the output circuit 100. The output circuit 200 includes the PVT compensating circuit 106 and the variable output drive 108. The output circuit 200 further includes a primary output drive 202, an impedance resistance 204, and an electrostatic discharge ("ESD") resistance 206. The primary drive 202 propagates the data signal 112 to the output terminal 104 through the impedance resistance 204. The PVT compensating circuit 106 monitors the output signal 120 at the output terminal 104, through the ESD resistance 206. In an embodiment, the ESD resistance 206 is part of an ESD circuit that protects the PVT compensating circuit 106 from ESD events that occur at the output terminal 104.

[0032] The PVT compensating circuit 106 monitors and/or senses one or more circuit and/or signal characteristics at the output terminal 104 and determines whether compensation is needed to correct for PVT variations in the IC core 110, the output circuit 200, and/or the load 114. For example, where the PVT compensating circuit 106 monitors changes in voltage with respect to time, the compensating circuit 106 determines whether the rate of change is within a desired or predetermined range. The PVT compensating circuit 106 generates the control signal 116 to increase, decrease, or maintain the rate of voltage change at the output terminal 104. The control signal 116 is provided to the variable output drive 108.

[0033] In an embodiment, the variable output drive 108 provides compensation to the output terminal 104 during state transitions of the output signal 120. In order to determine when state transitions occur, the variable output drive 108 also receives the data signal 112. The variable output drive

108 uses the data signal 112 as an enable signal to insure that the variable output drive 108 compensates during state transitions, as now described.

[0034] In FIG. 2, the variable output drive 108 includes a delay 208 that delays the data signal 112 by approximately the same amount of delay imparted on the data signal 112 as it is propagated from the IC core 110, to the output terminal 104, to the output of the PVT compensating circuit 106. The delay 208 allows the variable output drive 108 to determine whether the output signal 120, as viewed at the output terminal 104, is transitioning between states. When the signal at the output terminal 104 is transitioning between states, the variable output drive 108 is enabled to generate and/or adjust the compensation output signal 118. In an embodiment, the variable output drive 108 outputs the compensation output signal 118 to maintain, increase and/or decrease the rate of voltage change at the output terminal 104.

[0035] In an embodiment, the primary output drive 202 and the variable output drive 108 are current sources, which can be combined directly with one another.

II. Example Embodiments

[0036] FIG. 3A is a circuit diagram of an example output circuit 300 in accordance with an aspect of the present invention. The output circuit 300 is an example embodiment of the output circuit 200. The output circuit 300 includes a first set of compensation circuitry for compensating rising edges, generally denoted with the suffix "a" and a second set of compensation circuitry for compensating falling edges, generally denoted with the suffix "b."

[0037] In the output circuit 300, the primary output drive 202 includes primary output drives 202a and 202b, which drive positive and negative transitions (i.e., rising and falling edges), respectively. The primary output drive 202a is illustrated with an inverter 310a and one or more PMOS devices 312a. The primary output drive 202b is illustrated with an inverter 310b and one or more NMOS devices 312b. The invention is not, however, limited to

this embodiment. Other embodiments utilize other types and/or numbers of devices.

[0038] In the output circuit 300, the PVT compensating circuit 106 includes a feedback circuit 302 coupled to the ESD resistance 206. The feedback circuit 302 receives the output signal 120 from the output pad 104 through the ESD resistance 206. Alternatively, the feedback circuit 302 includes an internal resistance in place of, or in addition to the ESD resistance 206. The feedback circuit 302 generates a signal 304 representative of voltage ("V") or changes in voltage with respect to time ("dV/dt"), as measured at the output pad 104. In an embodiment, the feedback circuit 302 includes a capacitance that, when combined with the resistance of the ESD resistance 206, generates the V or dV/dt signal 304. In series with the capacitor, the feedback circuit 302 includes an inverter.

[0039] The feedback circuit 302 can be implemented in a variety of ways. For example, in FIG. 4, the feedback circuit 302 is implemented as an inverter. In FIG. 5, the feedback circuit 302 is implemented as a cross-coupled pair. The cross-coupled pair of FIG. 5 works similar to the inverter of FIG. 4. In FIGS. 6, 7, and 8, the feedback circuit 302 is implemented as voltage comparator circuits. In the voltage comparator circuits of FIGS. 6 and 7, the voltage from the output pad 104 is compared to a reference voltage (V_ref). When V_pad>V_ref, the current drive of the output circuit is reduced. When V_pad<V_ref, the current drive of the output circuit is increased. Typically, V_ref is close to VDDO/2 and could be generated by using a resistive divider on VDDO (as shown in FIG. 8) or other supply voltage. Other similar circuitry such as a current comparator could also be used instead of the voltage comparator. The invention is not, however, limited to these exemplary embodiments. Based on the description herein, one skilled in the relevant art(s) will understand that other circuit implementations of the feedback circuit 302 are possible. Such other implementations are within the scope of the present invention.

[0040] Referring back to FIG. 3, the PVT compensating circuit 106 generates separate control signals 116a and 116b for controlling compensation to rising and falling edges, respectively. The PVT compensating circuit 106 generates the rising edge control signal 116a with PMOS device 308a and NMOS device 306a. The PMOS device 308a acts as an adjustable voltage source that outputs the control signal 116a under control of the V or dV/dt signal 304. The NMOS device 307a acts as an enabling device that enables the V or dV/dt signal 304 to control the NMOS device 306a during state transitions of the output signal 120, and essentially terminates the V or dV/dt signal 304 when the output signal 120 is below a pre-determined value. The PVT compensating circuit 106 generates the falling edge control signal 116b in a similar fashion, using an NMOS device 308b and a PMOS device 306b.

[0041] In FIG. 3, the variable output drive 108 is illustrated with separate fingers for positive and negative transitions. Positive transitions are compensated with drive from a set of one or more PMOS devices 314a, under control of the control signal 116a. Negative transitions are compensated with drive from a set of one or more NMOS devices 314b, under control of the control signal 116b.

[0042] Impedance matching features of the invention are now described. In the primary output drive 202, the PMOS device(s) 312a and the NMOS device(s) 312b include inherent resistances and capacitances. Similarly, in the variable output drive 108, the PMOS device(s) 314a and the NMOS device(s) 314b include inherent resistances and capacitances. These inherent resistances and capacitances, together with the impedance resistance 204, form an output impedance. The PMOS devices 312a and 314a, the NMOS devices 312b and 314b, and the impedance resistance 204, are selected to provide an output impedance appropriate for a given load impedance.

[0043] In an embodiment, the impedance matching characteristics provided by the primary output drive 202 and the variable output drive 108 are relatively fixed without regard to the level of compensation provided by the variable output drive 108. Alternatively, under ideal or near-ideal circumstances (e.g.,

no PVT variations), when no compensation is required, the primary output drive 202 provides suitable impedance matching to the load 114. For non-ideal circumstances (e.g., PVT variations), the variable output drive 108 provides additional impedance matching characteristics. In an embodiment, the additional impedance matching characteristics of the variable output drive 108 vary in proportion to control signals 116a and 116b.

[0044] In operation, the output pad 104 is driven by fingers of devices 312a (e.g., MPd0-MPd3), 312b (e.g., MNd0-MNd3), 314a (e.g., MPd4-MPd17), and 314b (e.g., MNd4-MNd17). The value of the impedance resistance 204 (i.e., R_imp), is chosen such that the combination of the impedance resistor 204 and the inherent impedance of devices 312a, 312b, 314a, and 314b, match the impedance of the load 114. The voltage and dV/dt (change in voltage with time) at output pad 104 are fed-back to the PVT compensating circuit 106 after passing through the ESD resistance 206 (i.e., R_esd). The fed-back voltage and dV/dt are used to control the gate drives of the NMOS device 306a and the PMOS device 306b. The voltage level at the pad terminal and the rate of change of voltage at the pad terminal affects the switching-point of the input of the PVT compensating circuit 106.

[0045] The ESD resistor 206, along with input gate capacitance of the PVT compensating circuit 106, make the PVT compensating circuit sensitive to the dV/dt of the signal at the output pad 104. Thus, during rising transitions at the output pad 104, a high voltage at the output pad 104 and a high dV/dt causes the input of the PVT compensating circuit 106 (e.g., an inverter in FIG. 4), to be charged high fast causing the input NMOS device 404 to turn-on hard and fast, thereby quickly decreasing the gate voltage of the NMOS device 306a and PMOS device 308a to reduce the conduction of the NMOS device 306a and increase the conduction of the PMOS device 308a. This increases the voltage at 116a thereby reducing conduction of output PMOS 314a. Similarly, during falling transitions at the output pad 104, a low voltage at the output pad 104 and a high -dV/dt (high dV/dt in the negative direction), causes the PMOS device 402 to turn-on hard and fast, thereby quickly increasing the gate

voltage of the PMOS device 306b and NMOS device 308b, to reduce the conduction of the PMOS device 306b and increase conduction of the NMOS device 308b. This decreases the voltage at 116b, thereby reducing conduction of output NMOS device 314b. The voltage at the output pad 104 generally depends on the relative values of the impedance of the load 114 and the output transistors plus any built-in-resistor impedance.

[0046] In FIGS. 3-8, the PMOS device 308a and the NMOS device 308b are controlled by a single feedback circuit 302. Alternatively, the PMOS device 308a and the NMOS device 308b can also be controlled with separate feedback circuits.

[0047] In an embodiment, multiple PVT compensating circuits having varying switching points are used to control different legs of output PMOS and NMOS devices, each output PMOS and NMOS device coupled to different variable output drive fingers. This provides, among other things, greater granularity of control.

III. Methods of Operation

[0048] In FIG. 9 illustrates a process flowchart 900 for implementing the present invention. For exemplary purposes, the process flowchart 900 is described below with reference to one or more of the example system implementations illustrated in one or more of the drawing FIGS. 1-8. The present invention is not, however, limited to the example system implementations illustrated in drawing FIGS. 1-8. Based on the description herein, one skilled in the relevant art(s) will understand that the process flowchart 900 can be implemented with other system implementations as well. Such other implementations are within the spirit and scope of the present invention.

[0049] The process begins with step 902, which includes receiving an output signal from a circuit. For example, in FIG. 1, the data signal 112 is received at the input terminal 102.

[0050] Step 904 includes propagating the output signal to an output terminal. For example, in FIG. 2, the data signal 112 is propagated to the output terminal 104 by the primary output drive 202.

[0051] Step 906 includes sensing changes in voltage level and change in voltage with respect to time at the output terminal. For example, in FIG. 2, the PVT compensating circuit 106 senses changes in voltage with respect to time at the output terminal 104.

[0052] Step 908 includes generating a control signal proportional to the sensed changes in voltage with respect to time. For example, in FIG. 2, the PVT compensating circuit 106 generates the control signal 116 proportional to the sensed changes in voltage with respect to time.

[0053] Step 910 includes generating a supplemental drive signal under control of the control signal. For example, in FIG. 2, the variable output drive 108 generates the supplemental drive signal 118 under control of the control signal 116.

[0054] Step 912 includes providing the supplemental drive signal to the output terminal, wherein the output signal at the output terminal has a rate of voltage change with respect to time that is substantially within a predetermined range. For example, in FIG. 2, the supplemental drive signal 118 is combined with the output of the primary output drive 202 and provided to the output terminal 104 through the impedance resistance 204. The supplemental drive signal 118 is generated so as to substantially maintain the rate of voltage change at pad terminal 104 with respect to time within a predetermined range.

[0055] Step 914 includes impedance matching the output signal and said supplemental output signal to the load. For example, in FIG. 3, in an embodiment described above, the primary output drive 202 and the variable output drive 108 include inherent gate resistances and capacitances that, in combination with the impedance resistance 204, substantially matches the impedance of the load 114.

[0056] In an embodiment, the control signal generated in step 908 is further used to control impedance matching characteristics. For example, in FIG. 3, in

an embodiment, the inherent resistance of the variable output drive 108 varies in accordance with the control signal 116. As a result, the output signal 120 at the pad terminal 104 is substantially impedance matched to the load 114 for a range of process, voltage, and/or temperature variations in the circuits 110 and 300, and the load 114. Accordingly, FIG. 9 includes an optional step 916, which includes controlling the impedance matching with the control signal, wherein the output signal and the supplemental output signal are substantially impedance matched to the load for a range of process, voltage, and/or temperature variations in the circuit and the load.

IV. Conclusions

[0057] The present invention has been described above with the aid of functional building blocks illustrating the performance of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed. Any such alternate boundaries are thus within the scope and spirit of the claimed invention. One skilled in the art will recognize that these functional building blocks can be implemented by discrete components, application specific integrated circuits, processors executing appropriate software, and the like, and/or combinations thereof.

[0058] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.